AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A method for complex image rejection filtering in a direct sampling mixer comprising the steps of:

sampling an RF input with multiple phases of a local oscillator clock, each of the local oscillator phases producing a discrete-time signal stream; and

processing the multiple phases of the discrete-time signal in multiple paths, the paths sharing among themselves the discrete-time samples, whereby a bandpass filter characteristic is achieved during the processing step, and whereby an RF image is substantially rejected.

2. (Currently amended) A method according to claim 1 wherein the multiple phases of the local oscillator clock comprise at least two phases I and Q spaced approximately 90 degrees apart.

3. (Original) A method according to claim 1 wherein the multiple phases of the local oscillator clock consist of four phases I+, I-, Q+, Q-, spaced approximately 90 degrees apart.

4. (Original) A method according to claim 1 wherein the discrete-time signal stream comprises charge packets.

5. (Original) A method according to claim 1 wherein the step of sharing discrete-time samples further comprises the sharing of charge packets.

6. (Original) A method according to claim 1 further comprising the step of converting an RF input voltage into current.

7. (Currently amended) A method for complex filtering in a direct sampling mixer comprising:

sampling an RF input with I and Q phases of a local oscillator clock, each of the phases producing a stream of charge packets[[,]];

processing the I and Q charge packets in separate signal processing paths[[,]]; and

sharing the I and Q charge packets between the signal processing paths, whereby a bandpass filter characteristic is achieved during the processing step, and whereby an RF image is substantially rejected.

8. (Original) A complex filter system for filtering a high frequency input signal, the complex filter comprising:

a first IIR filter for sampling an I+ phase of the input signal;

a second IIR filter for sampling an I- phase of the input signal;

a third IIR filter for sampling an Q+ phase of the input signal;

a fourth IIR filter for sampling an Q- phase of the input signal;

wherein the IIR filters are interconnected for rotation of filtered signals such that in combination the interconnected IIR filters provide a complex filter.

9. (Currently amended) A complex filter system for filtering a high frequency input signal according to claim 8 wherein each IIR filter further comprises a history capacitor, rotating capacitor, and buffer capacitor adapted for sampling, storing and transferring charge from the input signal; and

wherein each IIR filter has a pole substantially determined by the ratio of its rotating capacitor to its history capacitor and is adapted to provide filtering of an input signal.

10. (Original) A complex filter system for filtering a high frequency input signal comprising:

two or more complex filter stages according to claim 8 coupled in a cascading configuration for providing high order filtering.

11. (Original) A complex filter system according to claim 10 further comprising one or more transconductive elements coupled between adjacent stages.

12. (Original) A complex filter system according to claim 10 further comprising one or more amplifier elements coupled between adjacent stages.

13. (Original) A complex filter system according to claim 10 further comprising one or more buffer elements coupled between adjacent stages.

14. (Currently amended) A complex filter system according to claim 9 wherein the system has a pole described by,

$C_H / (C_H + C_R) + j [C_R / (C_H + C_R)]$, ~~[Expression 2],~~ wherein;

C_R = rotating capacitor;

C_H = history capacitor.

15. (Original) A complex filter system according to claim 8 wherein the complex filter comprises a loop filter in a sigma-delta analog-to-digital converter.

16. (Currently amended) A circuit for image rejection filtering in a direct sampling mixer comprising:

an input node,

four parallel output nodes for producing four phases of an output signal;

coupled to the input node, ~~an~~ multiple IIR filters, each filter further comprising:

a buffer capacitor for buffering input current;

rotating capacitors coupled to the buffer capacitors in a configuration for reading the phase signal components in rotation and for providing mixed filtered phase signal component outputs to the output nodes.

17. (Original) A circuit according to claim 16 wherein the direct sampling mixer comprises a sigma-delta analog-to-digital converter.

18. (Original) A circuit for image rejection filtering in a direct sampling mixer comprising two or more circuit stages according to claim 16 coupled in a cascaded configuration.

19. (Original) A circuit for image rejection filtering in a direct sampling mixer according to claim 18 further comprising one or more transconductive elements coupled between adjacent stages.

20. (Original) A circuit for image rejection filtering in a direct sampling mixer according to claim 18 further comprising one or more amplifier elements coupled between adjacent stages.

21. (Original) A circuit for image rejection filtering in a direct sampling mixer according to claim 18 further comprising one or more buffer elements coupled between adjacent stages.